EP 703 716 (A)

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 703 713 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
27.03.1996 Bulletin 1996/13

(51) Int Cl.[6]: **H04N 7/58**

(21) Application number: **95306655.2**

(22) Date of filing: **20.09.1995**

(84) Designated Contracting States:
DE FR GB

(30) Priority: **22.09.1994 JP 254687/94**

(71) Applicant: **SONY CORPORATION**
Tokyo 141 (JP)

(72) Inventor: **Shiga, Tomohisa**
Shinagawa-ku, Tokyo 141 (JP)

(74) Representative:
Ayers, Martyn Lewis Stanley et al
J.A. KEMP & CO.
14 South Square
Gray's Inn
London WC1R 5LX (GB)

(54) Packet receiving device

(57) An apparatus for receiving and decoding a packet of a multiplexed stream whose data are coded to a predetermined format, including temporary storing means for compensating for the difference between the timing of the received packet and the read-in timing of the coded data by a decoder, means for producing a clock signal serving as a reference to operate the decoder on the basis of a reference signal in the format, and means for calculating the position of the reference signal using a time which is periodically added to the packet.

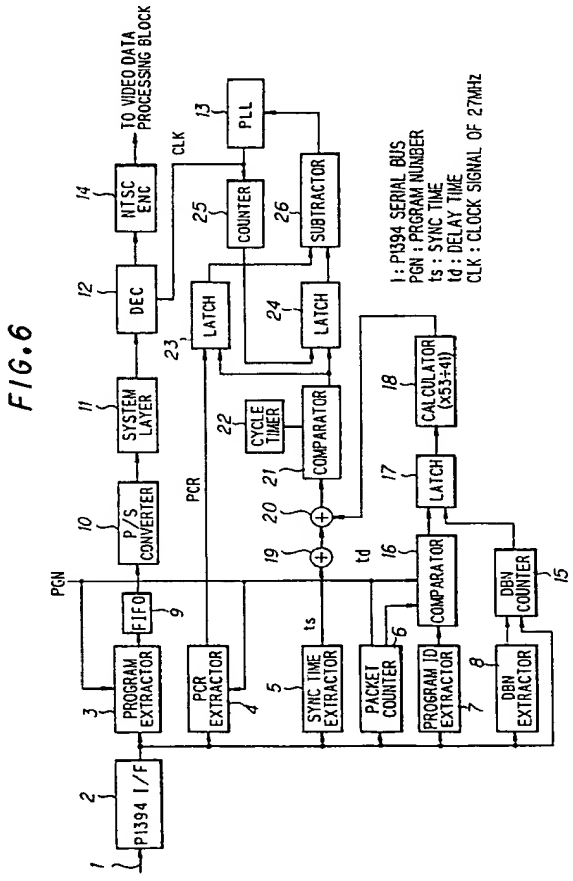


FIG.6

EP 0 703 713 A2

Printed by Jouve (FR), 18, rue Saint-Denis, 75001 PARIS

BNSDOCID: <EP_____0703713A2_I_>

Description

The present invention relates to a device for receiving and reproducing packet data having a multiplexed transport stream, in particular, but not exclusively of MPEG by using a communication control bus which is based on the IEEE- P1394 (hereinafter referred to "P1394 serial bus").

There has been hitherto proposed a system in which plural equipments are connected to one another through a P1394 serial bus and communication is performed among these equipments.

Fig. 1 of the accompanying drawings shows such a system as described above. The system includes three digital video tape recorders (VTR 1 to 3), a digital cam corder (CAM), and a digital television receiver (FTV1). These equipments are connected to one another through a P1394 serial bus cable. Each equipment has a function of relaying an information signal and a control signal which are input from the P1394 serial bus cable, so that the communication system is equivalent to a communication system in which the respective equipments are connected to a common P1394 serial bus.

Data transmission of the equipments having the common bus is performed in a time-divisional multiplexing mode every predetermined communication cycle (125μsec, for example) as shown in Fig.6. The communication cycle on the bus is managed by a predetermined equipment which is called as "cycle master", and the data transmission of a communication cycle is started in synchronism with transmission of a synchronizing packet representing the start time of the communication cycle (cycle start packet) from the cycle master to another equipment on the bus. The operation of the cycle master is automatically determined by a method defined in IEEE-P1394 when respective equipments are connected through a P1394 serial bus to construct a communication system.

As a type of data transmission in a communication cycle are provided two types of data, synchronized type (Isochronous) data such as video data, audio data, etc., and non-synchronized (Asynchronous) data such as connection control commands, etc. The isochronous data packets is transmitted prior to the asynchronous data packets. Plural isochronous data can be discriminated from one another by numbering the respective isochronous data packets with channel numbers 1, 2, 3, ..., N. The asynchronous data packets are transmitted for a period from the end of the transmission of the isochronous data packets of all channels to be transmitted until a next cycle start packet.

In the communication system thus constructed, the case will now be considered that MPEG transport packets of plural programs are transmitted while multiplexed in an isochronous data packet of one channel.

As shown in Fig. 3, the MPEG transport packet has a length of 188 bytes, and it comprises a link header, an adaptation header and a pay-load (data portion). The link header is provided with a program ID. The adaptation header is provided with Program Clock Reference (hereinafter referred to as "PCR") from a position corresponding a second byte from the head thereof.

The program ID is a code for identifying a program, and PCR serves as a reference (time base) for an extracting time of data of each program at a reception side when the stream of the MPEG transport packets of plural programs is transmitted while multiplexed in an isochronous data packet of one channel. When it is required to receive a desired program, at the reception side an MPEG transport stream is formed from the isochronous data packet which is received through the P1394 serial bus, PCR corresponding to the desired program is read out from the transport stream, and a PLL for generating clock signals of 27MHz to be supplied to an MPEG decoder is locked.

However, this method needs two PLLS, one of which is to generate clock signals to read out a transport stream, and the other of which is to generate clock signals of 27Mhz to be output to the decoder. Furthermore, this method further needs totally two FIFOs, one of which is to form a transport stream from a received isochronous data packet, and the other of which is to compensate for the difference between the timing of the transport stream and the data read-in timing of the decoder. The following eight relating applications have been filed by the same applicant:

1. European Laid-open Application No: 0614297
2. Japanese Application No.: 05126682
3. Japanese Application No.: 05200055
4. Japanese Application No.: 06051246
5. Japanese Application No.: 06134940
6. Japanese Application No.: 06165883
7. Japanese Application No.06192807
8. Japanese Application No.: 06242255

The corresponding U.S. Applications to these applications are now pending in U.S.

An object of the present invention is to provide an improved packet receiving device, in particular but not exclusively, for decoding a transport stream of MPEG having plural multiplexed programs by a single PLL and a single FIFO.

According to the present invention, there is provided an apparatus for receiving and decoding a packet of a multiplexed stream whose data are coded to a predetermined format, including:

temporary storing means for compensating for the difference between the timing of the received packet and

BNSDOCID: <EP_____0703713A2_I_>

the read-in timing of the coded data by a decoder;

means for producing a clock signal serving as a reference to operate the decoder on the basis of a reference signal in the format; and

means for calculating the position of the reference signal using a time which is periodically added to the packet.

The data stream of a single program extracted from the received packet is written in the temporary storing means. The data stream extracted from the received packet is supplied to the decoder through the temporarily storing means.

Furthermore, the means of producing the clock signal to operate the decoder can be constituted so as to require a single PLL. The means of calculating the position of the reference signal may comprise first means for calculating the time difference from the time until the reference signal on the basis of the position information in the predetermined format of the data extracted from the received packet and the periodical position information in the stream, and second means for converting the time difference into the number of clocks in a transmission path.

The second means may comprise a first counter for counting the clock signal of the data stream, a second counter for counting the clock signal in the transmission path, and a latch for latching the output value of the second counter when the time difference calculated by the first means is coincident with the output value of the first counter.

According to an embodiment of the present invention, the difference between the timing of the received packet and the data read-in timing of the decoder is compensated by the temporary storing means. The clock signal to operate the decoder is produced on the basis of the reference signal of the predetermined format which is extracted from the received packet. The position of the reference signal is calculated using the time which is periodically added to the packet.

Therefore, at the reception side the reference signal can be read out and the clock signal to operate the decoder can be produced without reproducing the stream of the data which are coded to the predetermined format. Accordingly, PCR can be read out from the MPEG transport stream transmitted using a P1394 serial bus without reproducing the transport stream at the reception side, thereby producing clock signals of 27MHz for operating the decoder.

Furthermore, according to the present invention, the reception of the packet of the multiplexed stream of the data which are coded to the predetermined format at a transmission side and the decoding of the data can be performed by a receiving device having a single temporarily storing means and a single PLL.

The invention will be further described by way of non-limitative example with reference to the accompanying drawings, in which:-

Fig. 1 is a diagram showing a communication system using a P1394 serial bus;

Fig. 2 is a diagram showing a communication cycle in the P1394 serial bus;

Fig. 3 is a diagram showing a transport packet of MPEG;

Fig. 4 is a diagram showing a timing of a signal at a transmission side in an embodiment according to the present invention.

Fig. 5 is a diagram showing a timing of a signal at a reception side in the embodiment according to the present invention.

Fig. 6 is a block diagram showing a receiving device in the present invention; and

Fig. 7 is a block diagram showing a modification of the receiving device of the present invention.

An embodiment in which a transport stream of 19.3MHz having five multiplexed programs is transmitted with an isochronous data packet of P1394 serial bus, and received to extract an indicated program from the received transport stream and convert it to a video signal of NTSC system will be described in the following item order:

(1) Timing of Transmission side,

(2) Timing of Reception side,

(3) Receiving Device and

(4) Modification of Receiving Device

(1) Timing of Transmission side

The timing of the transmission side will be described with reference to Fig. 4. In Fig. 4, (a) represents an input transport stream, (b) represents data block numbers (which will be described in detail later, and is hereinafter referred to as "DBN"), and (c) represents a packet to be transmitted.

In the P1394 serial bus, a packet is output every 125μs as shown in Fig. 4, and the input transport stream is transmitted while packetted every 125μs as a packet unit. In this embodiment, a transport stream which is written in an FIFO (not shown) of a transmission device during a cycle T1 is transmitted as a packet P1, and a transport stream which is written during a cycle T2 is transmitted as a packet P2.

It is usually favourable in the P1394 serial bus that data are transmitted every one quadrate (32 bits), and thus the input transport stream is converted to parallel

BNSDOCID: <EP_____0703713A2_I_>

data of one quadrate by a serial/parallel converter in the transmitting device. (a) of Fig. 4 shows a transport stream after converted to parallel data of one quadrate.

Each of all packets which are transmitted by the P1394 serial bus is provided with packet length and DBN. In this embodiment, the input transport stream is assumed to be a virtual assembly of bit array which is repeated at a constant cycle. That is, a transport stream which realistically has no constant cycle or is repeated at different cycles is regarded as an assembly of bit array which is repeated at a constant cycle, and virtually framed. The framing of the transport stream is performed with a counter which operates at the same rate as the bit rate of the input transport stream. The output value of the counter corresponds to DBN shown in (b) of Fig. 4. DBN represents the output value of the counter for counting quadrate , which is written at the head of each packet.

There are two groups of packets, each packet of one group being provided with a sync time (Sync Time) while each packet of the other group is provided with no sync time. The provision of the sync time to a packet is determined on the basis of judgment as to whether data having "0" as DBN are contained in data which are transmitted by the packet. The sync time is defined as a time which is indicated by a cycle timer of P1394 when DBN is equal to zero. The cycle timer is provided in each equipment, and it has a time which makes a round at a predetermined cycle (128 seconds, for example).

The clock signals at the transmission side and the reception side are independent of each other, and are not synchronous with each other, so that an error between the clock signals is accumulated and a time lag is gradually increased between the write-in rate of the bit stream into the FIFO at the transmission side and the read-out rate of the bit stream from the FIFO at the reception side. The sync time is used as information to adjust this time lag.

Only one sync time must be provided in one packet, and thus the counter which performs the framing must be set to be longer than the cycle of P1394 (125μs). In this embodiment, a counter whose cycle is substantially equal to 167μs, for example, a counter which makes a round by counting a clock signal of 600kHz at 100 times is used.

During the cycle T1 in Fig. 4, DBN is equal to zero, so that a sync time is provided to the packet P1. Likewise, since DBN is equal to zero during the cycle T3, a sync time is provided to the packet P3. However, DBN is not equal to zero during the cycle T, no sync time is provided to the packet P2.

[2] Timing of Reception Side

Next, the timing of the reception side will be described with reference to Fig. 5. In Fig. 5, (a) represents a received packet, (b) represents a virtual transport stream, (c) represents an output value of a counter for outputting DBN, and (d) represents an output value of a packet counter. (a), (b) and (d) are associated with the time axis direction, however, (b) is not associated with the time axis direction.

The reception side is provided with a counter for outputting DBN (hereinafter referred to as "DBN counter") and a counter for indicating the position of a transport packet in the received packet. The output values of these counters are shown in (c) and (d) of Fig. 2, respectively.

Upon reception of a packet, DBN and the output value of the packet counter are incremented by "1" every time data of one quadrate are read out from the packet. Since the cycle of DBN is equal to 100, a value next to 99 is equal to zero. The output value of the packet counter which is subsequent to 46 is equal to zero. This is because the length of the transport packet is set to 47 quadrates (188 bytes) by MPEG.

When DBN is read out from the received packet, the output value of the DBN counter is forcedly set to DBN which is written in the packet. For example, DBN=99 is written in the packet P4 of Fig. 5, so that the DBN counter is forcedly set to 99. If the DBN counter operates normally, the output value of the DBN counter would be set to 99 at the time when receiving DBN of the packet P4.

At the reception side, a time at which the PCR as described above should be reproduced is calculated using the output value of the DBN counter, the output value of the packet counter and the sync time to reproduce a clock signal of 27MHz which is coincident with that at the transmission side. This calculation method will be described below.

First, the program ID of the transport stream is read out, and it is checked whether a currently read-out program is an indicated program. If it is judged to be the indicated program, the value of DBN at which the output value of the packet counter is equal to 1 is read out. This is because PCR is written at a second quadrate position of the transport packet as shown in Fig. 7.

The value of the DBN counter at this time is equal to the number of quadrates from the sync time written in the received packet. Accordingly, if this value is multiplied by the length of one cycle of the clock signal which is synchronized with the transport stream, the period from the time indicated by the sync time until PCR can be calculated. Furthermore, by converting this time to the clock number at 24.576MHz of the reference clock signal of P1394 and adding the obtained value to the sync time, the time at which the PCR should be reproduced can be calculated. This situation is shown by the virtual transport stream shown in (b) of Fig. 5. The virtual transport stream is introduced for convenience's sake of the description, and actually the transport stream is not reproduced in the receiving device.

[3] Receiving Device

Next, the receiving device will be described with reference to the block diagram of Fig. 6. The receiving de-

BNSDOCID: <EP_____0703713A2_I_>

vice (the transmitting device as described above) is provided in each equipment in the case of the communication system as shown in Fig. 1. The output of the receiving device is transmitted to a video data processing block of each equipment.

The packet which is transmitted through the P1394 serial bus 1 is received by a P1394 interface (hereinafter referred to as "P1394 I/F") 2, and output to a program extraction circuit 3, a PCR extraction circuit 4, a sync time extraction circuit 5, a packet counter 6, a program ID extraction circuit 7 and a DBN extraction circuit 8.

The program extraction circuit 3 extracts a program indicated by a program number PGN, and writes it into an FIFO 9. The program which is written in the FIFO 9 is converted to a serial bit stream by a parallel/serial conversion circuit 10, and then output to a system layer processing block 11. The program is subjected to the processing in the system layer of MPEG, whereby the bit stream is converted to a format which is conformable to the decoder 12.

The decoder 12 reads data from the system layer processing block 11 in synchronism with the click signal of 27MHz which is input from the PLL 13, and outputs the data to an NTSC encoder 14. The NTSC encoder 14 outputs video signals of NTSC system to a video data processing block.

The DBN extraction circuit 8 extracts DBN from the packet, and outputs it to the DBN counter 15. When DBN is input from the DBN extraction circuit 8 to the DBN counter 15, the DBN is set in the DBN counter 15, and at the other times, the DBN counter 15 counts up every time the P1394 I/F 2 outputs data of one quadrate. The DBN counter operates at a cycle of 100.

The packet counter 6 outputs the current quadrate position of a transport packet indicated by the program number PGN from the transport stream in the received packet by performing the frame synchronization.

When the value of the packet counter 6 is equal to 1 and the output value of the program ID extraction circuit 7 is equal to the program number PGN, a comparison circuit 16 outputs a comparison result to a latch 17. As described above, the program ID is an inherent value which is provided every transport packet and also provided every program.

When receiving an input from the comparison circuit 16, the latch 17 latches the output value of the DBN counter 15 at that time, and outputs it to a calculation circuit 18. The DBN at this time is equal to the quadrate number from the time indicated by the sync time written in the received packet until the PCR.

In the calculation circuit 18, the above value is multiplied by 52ns which corresponds to one cycle of the clock signal synchronized with the transport stream, and divided by 41ns which corresponds to one cycle of 24.576MHz which is the reference clock signal of P1394 to convert the time until the PCR to the clock number in P1394.

The sync time extraction circuit 5 extracts a sync time ts from the transport packet, and outputs it to an adder 19. The adder 19 adds the sync time ts with a predetermined delay time td, and outputs the result to an adder 20. In this case, the delay time td is added to the sync time ts because the time of the sync time written in the packet corresponds to the time at the transmission side and thus it has already passed over the time of the sync time due to jitter ■T of the packet or the like at the time when the packet is received at the reception side and the data written in the packet are read out as a bit stream. The jitter inherently occurs when the P1394 serial bus is used.

The adder 20 adds the output of the adder 19 with the output of the calculation circuit 18, and outputs the addition result to a comparison circuit 21. The comparison circuit 21 compares the output values of the cycle timer 23 and the adder 20 with each other, and outputs the comparison result to latches 23 and 24 when the output values are equal to each other.

The PCR extraction circuit 4 extracts PCR which is located at the second quadrate position of the transport packet. The PCR extracted by the PCR extraction circuit 4 on the basis of the output of the comparison circuit 21 is latched by the latch 23, and the output of the counter 25 is latched by the latch 24. The counter 25 operates with the clock signal of 27MHz which is output by the PLL 13, and also operates according to the same algorithm as the PCR generated at the transmission side.

A subtraction circuit 26 calculates the different between the input values from the latch 23 and the latch 24, and outputs the difference to the PLL 13. A target to be latched by the latch 23 is the PCR which is prepared at the transmission side. On the other hand, a target to be latched by the latch 24 is the PCR which is prepared at the reception side. The PLL 13 adjusts the phase of the output clock signal in accordance with the output of the subtraction circuit 26 so that the output of the latch 24 is coincident with the output of the latch 23. With these processing, the phase of the PCR prepared in the counter at the reception side can be matched with the phase of the PCR prepared at the transmission side, so that synchronization can be established between the clock signal of the PLL 13 and the clock signal of the transmission side.

[4] Modification of Receiving Device

A modification of the receiving device will be described with reference to Fig. 7. In the following description, only the portion different from Fig. 6 will be described.

Like the latch 17 of Fig. 6, a latch 31 is input with the output of the DBN counter 15 and the output of the comparison circuit 16. The latch 31 outputs a latched value to a comparison circuit 32 and resets counters 34 and 35 in synchronism with its latch timing.

The counter 34 counts up with a clock signal of 19.3MHz which is synchronized with the transport

BNSDOCID: <EP_____0703713A2_1_>

stream of MPEG, and the counter 35 counts up with a clock signal of 24.576MHz which is a clock signal of P1394.

The comparison circuit 32 outputs a signal to the latch 33 when the output of the counter 34 and the output of the latch 31 are coincident with each other, and the latch 33 latches the output value of the counter 35 at that time. As a result, the output of the latch 33 is equal to the output of the calculation circuit 18 of Fig. 6.

According to this modification, the calculation of the calculation circuit 18 of Fig. 6 can be performed with a simple hardware. In addition, even when only a specific program is selected and transmitted at the transmission side, the same effect can be obtained.

Claims

1. An apparatus for receiving and decoding a packet of a multiplexed stream whose data are coded to a predetermined format, including:

   temporary storing means for compensating for the difference between the timing of the received packet and the read-in timing of the coded data by a decoder;

   means for producing a clock signal serving as a reference to operate the decoder on the basis of a reference signal in the format; and

   means for calculating the position of the reference signal using a time which is periodically added to the packet.

2. The apparatus as claimed in claim 1, wherein a data stream of a single program extracted from the received packet is written in said temporary storing means.

3. The apparatus as claimed in claim 2, wherein the data stream extracted from the received packet is supplied to the decoder through said temporary storing means.

4. The apparatus as claimed in claim 3, wherein said means of producing the clock signal to operate the decoder has a single PLL.

5. The apparatus as claimed in claim 4, wherein said means of calculating the position of the reference signal comprises first means for calculating the time difference from the time until the reference signal on the basis of the position information in the predetermined format of the data extracted from the received packet and the periodical position information in the stream, and second means for converting the time difference into the number of clocks in a transmission path.

6. The apparatus as claimed in claim 5, wherein said second means comprises a first counter for counting the clock signal of the data stream, a second counter for counting the clock signal in the transmission path, and a latch for latching the output value of said second counter when the time difference calculated by said first means is coincident with the output value of said first counter.

7. Apparatus according to any one of the preceding claims, and including an IEEE P1394 - compliant bus over which the multiplexed stream of data is communicated.

BNSDOCID: <EP_____0703713A2_I_>

FIG. 1

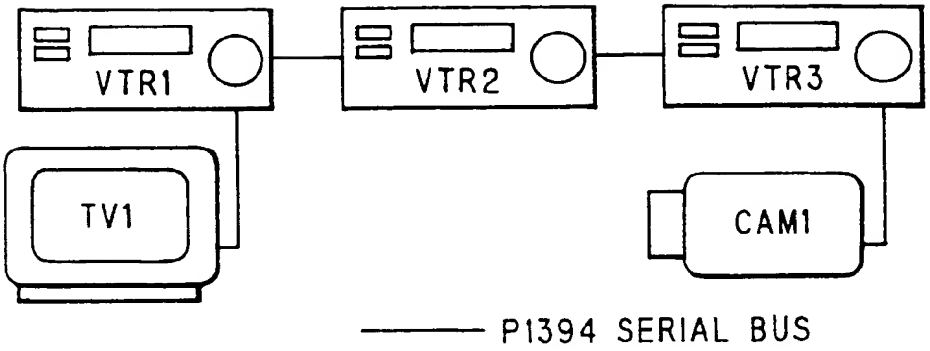
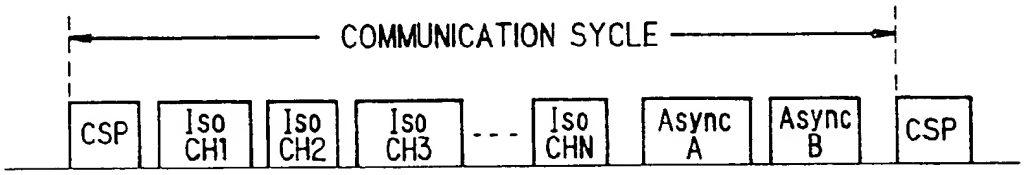
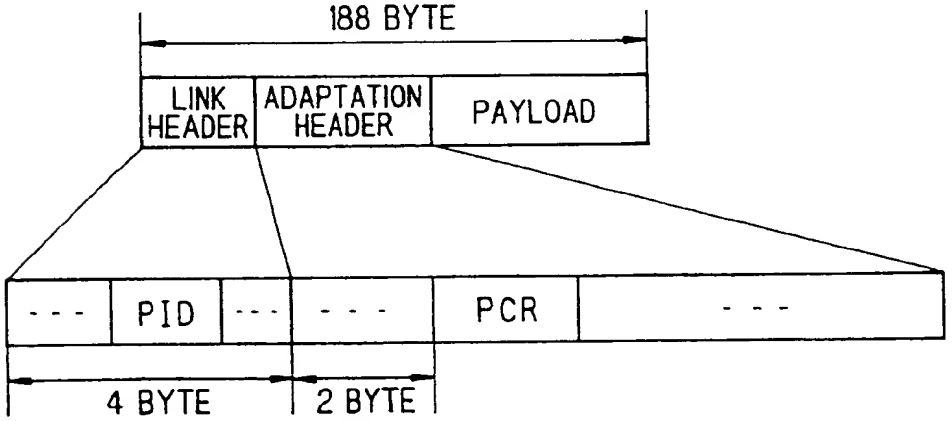


FIG. 2



CSP : CYCLE START PACKET
Iso : ISOCHRONOUS DATA PACKET
Async : ASYNCHRONOUS DATA PACKET

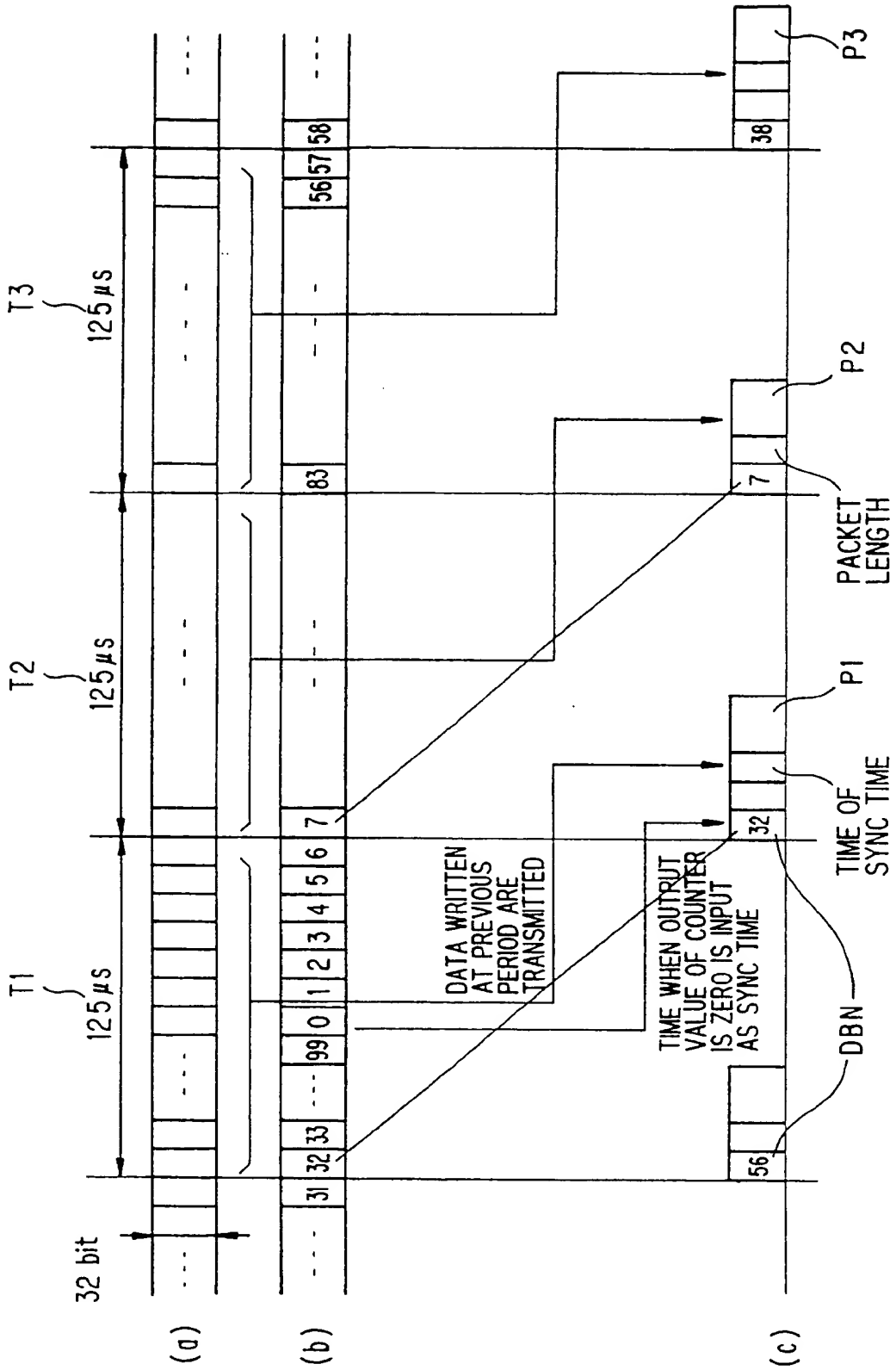
FIG. 3



PID : PROGRAM ID
PCR : Program Clock Reference

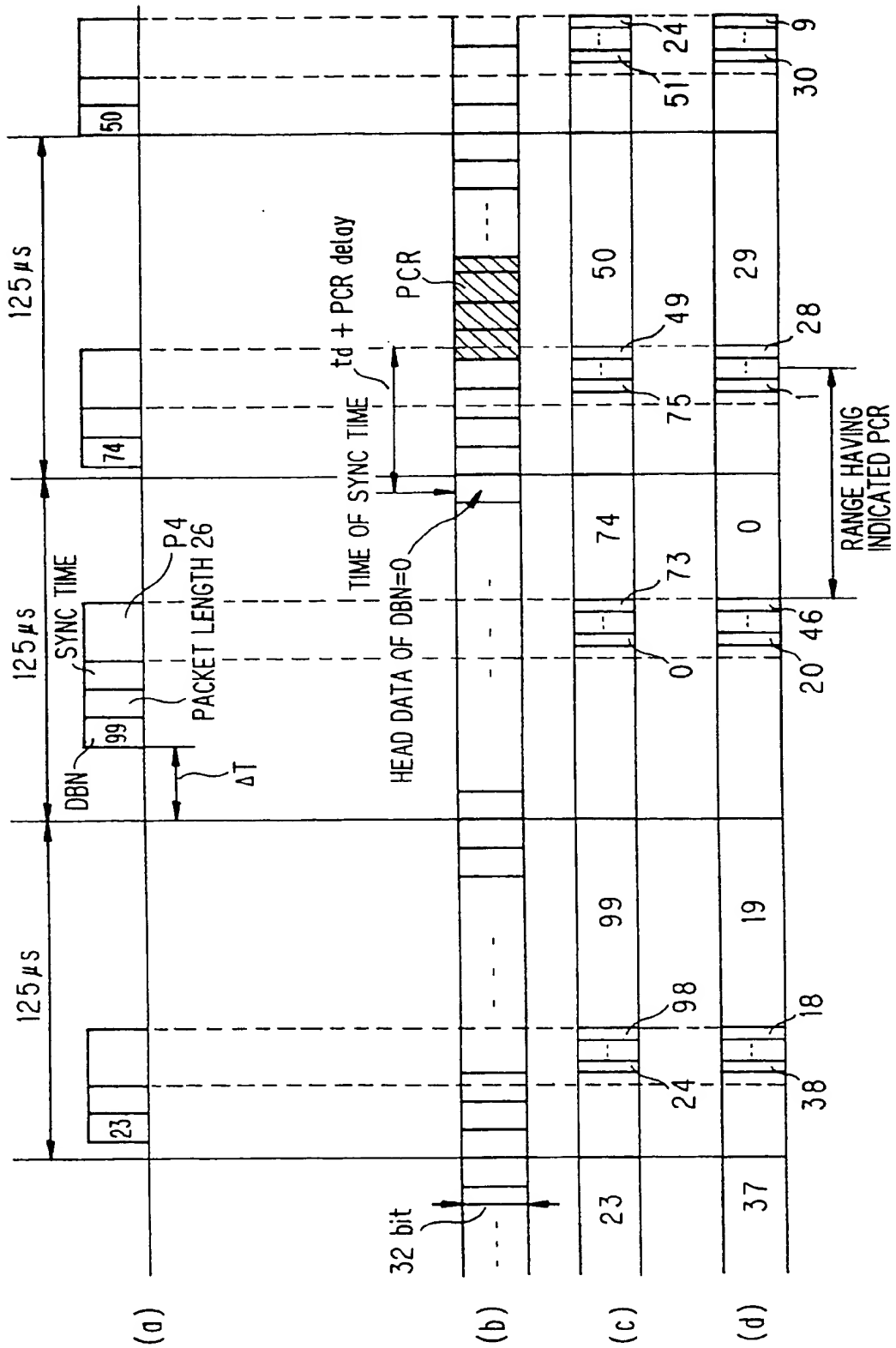
BNSDOCID: <EP_____0703713A2_I_>

FIG. 4



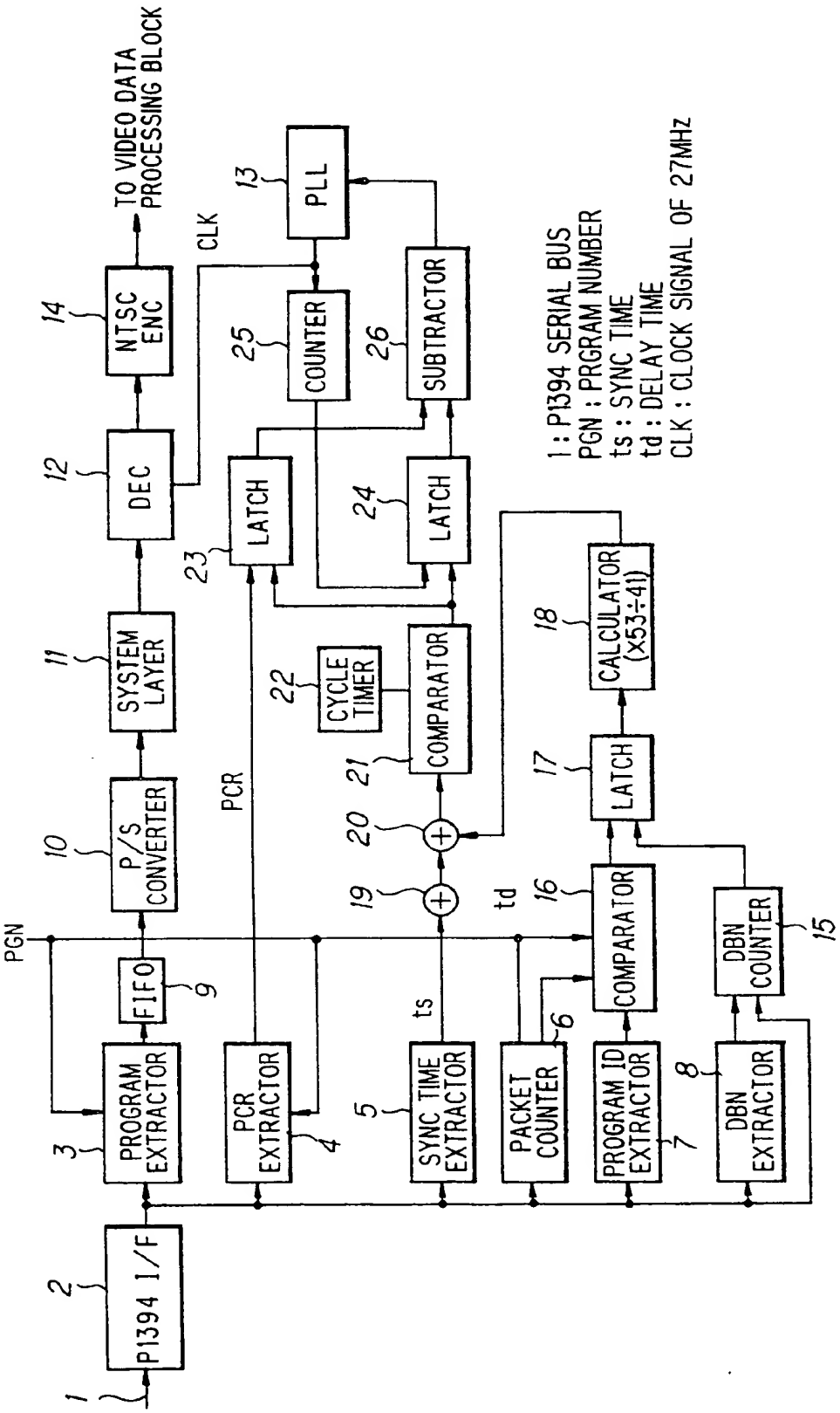
BNSDOCID: <EP_____0703713A2_I_>

FIG.5



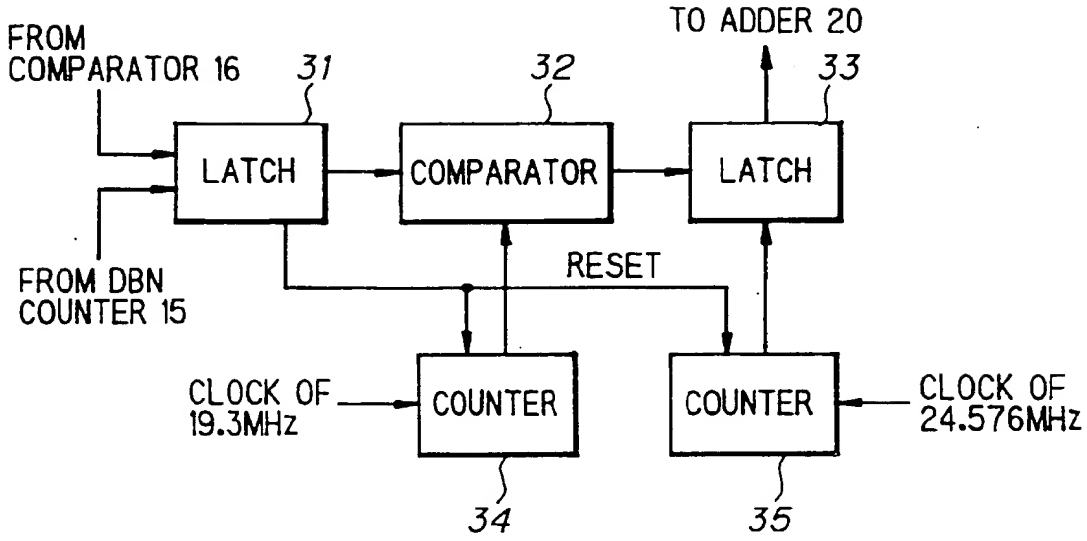
BNSDOCID: <EP_____0703713A2_I_>

FIG.6



BNSDOCID: <EP_____0703713A2_I_>

FIG. 7



BNSDOCID: <EP_____0703713A2_I_>

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 703 713 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
25.03.1998 Bulletin 1998/13

(43) Date of publication A2:
27.03.1996 Bulletin 1996/13

(21) Application number: **95306655.2**

(22) Date of filing: **20.09.1995**

(51) Int Cl.[6]: **H04N 7/58**, H04N 7/62

(84) Designated Contracting States:
DE FR GB

(30) Priority: **22.09.1994 JP 254687/94**

(71) Applicant: **SONY CORPORATION**
Tokyo 141 (JP)

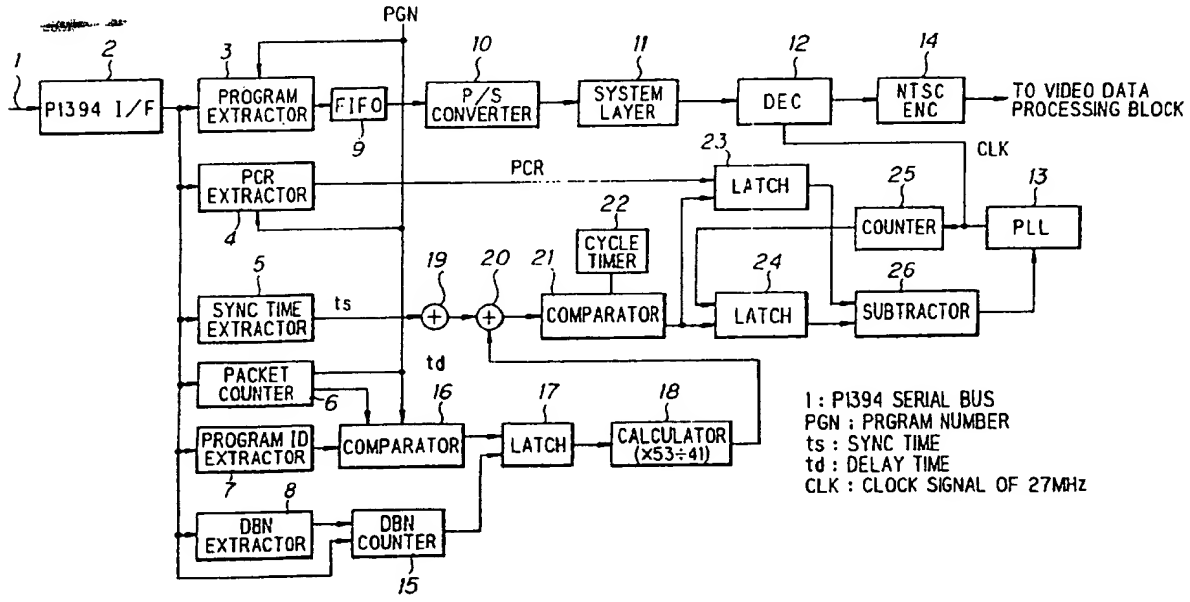
(72) Inventor: **Shiga, Tomohisa**
Shinagawa-ku, Tokyo 141 (JP)

(74) Representative: **Ayers, Martyn Lewis Stanley et al**
J.A. KEMP & CO.
14 South Square
Gray's Inn
London WC1R 5LX (GB)

(54) Packet receiving device

(57) An apparatus for receiving and decoding a packet of a multiplexed stream whose data are coded to a predetermined format, including temporary storing means for compensating for the difference between the timing of the received packet and the read-in timing of the coded data by a decoder, means for producing a clock signal serving as a reference to operate the decoder on the basis of a reference signal in the format, and means for calculating the position of the reference signal using a time which is periodically added to the packet.

FIG. 6



EP 0 703 713 A3

Printed by Jouve, 75001 PARIS (FR)

BNSDOCID: <EP_____0703713A3_I_>

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 6655

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 4 982 284 A (KOGA TOSHIO) * abstract * ---	1-3	H04N7/58 H04N7/62
X	"OPTIMIZED DATA TIME STAMPS FOR DIGITAL AUDIO AMD VIDEO ON A STOCHASTIC NETWORK" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 36, no. 9A, 1 September 1993, page 183 XP000395356 * the whole document * ---	1-3	
E	WO 95 27977 A (PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) * abstract * * page 28, line 8 - line 11 * * page 31, line 3 - line 23 * * page 32, line 16 - line 20 * * figures 18,22,23 * ---	1-4	
P,X	KUNZMAN A J ET AL: "1394 HIGH PERFORMANCE SERIAL BUS: THE DIGITAL INTERFACE FOR ATV" IEEE TRANSACTIONS ON CONSUMER ELECTRONICS, vol. 41, no. 3, August 1995, pages 893-900, XP000539552	1-3	
P,A	* page 898, right-hand column, line 27 - line 34 * * figure 6 * ---	4-7	
P,X	"TRANSMISSION OF AN MPEG ENCODED INFORMATION SIGNAL USING TIME STAMPS" RESEARCH DISCLOSURE, no. 375, July 1995, page 508 XP000524830	1-3	
P,A	* page 508, paragraph 5 * --- -/--	4-7	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 January 1998	Berbain, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

BNSDOCID: <EP_____0703713A3_I_>

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 6655

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	BURSKY D: "CHIP SET SIMPLIFIES HIGH-SPEED INTERCONNECTS THE FIST ICS TO REALIZE THE P1394 SERIAL-BUS STANDARD LET DESIGNERS BUILD SERIAL CONNECTIONS RUNNING AT 100 TO 400 MBITS/S" ELECTRONIC DESIGN, vol. 42, no. 5, 7 March 1994, pages 114-117, XP000441329 * page 116, left-hand column, line 5 - line 24 * ---	1-7	
A	TEENER M: "A BUS ON A DIET - THE SERIAL BUS ALTERNATIVE AN INTRODUCTION TO THE P1394 HIGH PERFORMANCE SERIAL BUS" INTELLECTUAL LEVERAGE, SAN FRANCISCO, FEB. 24 - 28, 1992, no. CONF. 37, 24 February 1992, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS. pages 316-321, XP000340753 * the whole document * -----	1-7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 January 1998	Berbain, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

BNSDOCID: <EP_____0703713A3_I_>